PATENT

This listing of the claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

Claims 11, 20, and 29 have been canceled. Claims 1-10, 12-19 and 21-28 are being amended as follows:

Sub B1

1. (currently amended) A charge pump circuit comprising:

a first native transistor;

~~a first capacitor coupled to the first transistor;~~

~~a second transistor coupled to the first transistor; and~~

~~a second capacitor coupled to the second transistor, wherein the second transistor has a lower threshold voltage than the first transistor at a common source voltage~~

first depletion transistors each having a threshold voltage that is lower that a threshold voltage of the first native transistor at a common source voltage, wherein the first native transistor and the first depletion transistors are coupled together in series between an input and an output of the charge pump circuit; and

first capacitors, wherein a drain of each of the first depletion transistors is coupled to one of the first capacitors, a first subset of the first capacitors are coupled to receive a first clock signal, and a second subset of the first capacitors are coupled to receive a second clock signal.

2. (currently amended) The charge pump circuit of claim 1 further comprising:

~~a third transistor coupled to the second transistor; and~~

~~a third capacitor coupled to the third transistor, wherein the third transistor has a lower threshold voltage than the first transistor at a common source voltage~~

second depletion transistors each having a threshold voltage that is lower than the threshold voltage of each of the first depletion transistors at a common source voltage,

wherein a drain of each of the second depletion transistors is coupled to one of the first capacitors, and

the first native transistor, the first depletion transistors, and the second depletion transistors are all coupled together in series between the input and the output of the charge pump circuit.

3. (currently amended) The charge pump circuit of claim 2 ~~further comprising:~~

a1

~~a fourth transistor coupled to the third transistor; and~~

~~a fourth capacitor coupled to the fourth transistor, wherein the fourth transistor has a lower threshold voltage than the first transistor at a common source voltage~~ wherein the first depletion transistors include at least four depletion transistors, and the second depletion transistors include at least four depletion transistors.

4. (currently amended) The charge pump circuit of claim 3 ~~further comprising:~~

~~a fifth transistor coupled to the fourth transistor; and~~

~~a fifth capacitor coupled to the fifth transistor, wherein the fifth transistor has a lower threshold voltage than the first transistor at a common source voltage~~

wherein the first depletion transistors include at least six depletion transistors, and the second depletion transistors include at least six depletion transistors.

5. (currently amended) The charge pump circuit of claim ~~3~~ 1 further comprising ~~four~~ diode-connected transistors, wherein each diode-connection transistor is coupled to a gate of one of the ~~first, second, third, and fourth~~ first depletion transistors.

6. (currently amended) The charge pump circuit of claim 4 ~~further comprising:~~

~~a sixth transistor coupled to the fifth transistor;~~

~~a sixth capacitor coupled to the sixth transistor;~~

~~a seventh transistor coupled to the sixth transistor;~~

~~a seventh capacitor coupled to the seventh transistor;~~

~~an eighth transistor coupled to the seventh transistor; and~~

~~an eighth capacitor coupled to the eighth transistor, wherein the sixth, seventh, and eighth transistors each have a lower threshold voltages than the first transistor at a common source voltage~~

wherein the first depletion transistors include at least seven depletion transistors, and the second depletion transistors include at least seven depletion transistors.

7. (currently amended) The charge pump circuit of claim 1 ~~6~~ further comprising:

~~a ninth transistor coupled to the eighth transistor;~~

~~a ninth capacitor coupled to the ninth transistor;~~

~~a tenth transistor coupled to the ninth transistor;~~

~~a tenth capacitor coupled to the tenth transistor;~~

~~an eleventh transistor coupled to the tenth transistor; and~~

~~an eleventh capacitor coupled to the eleventh transistor, wherein the ninth, tenth, and eleventh transistors each have a lower threshold voltages than the first transistor at a common source voltage~~

a second native transistor that is coupled in series with the first native transistor.

8. (currently amended) The charge pump circuit of claim ~~7~~ 2 ~~further comprising:~~

~~a twelfth transistor coupled to the eleventh transistor;~~

~~a twelfth capacitor coupled to the twelfth transistor;~~

~~a thirteenth transistor coupled to the twelfth transistor;~~

~~a thirteenth capacitor coupled to the thirteenth transistor, wherein the twelfth and thirteenth transistors each have a lower threshold voltages than the first transistor at a common source voltage~~

wherein each of the first depletion transistors have a negative threshold voltage implant region with a first concentration of an N-type dopant, and each of the second depletion transistors have a negative threshold implant region with a second concentration of the N-type dopant, the second concentration of the N-type dopant being greater than the first concentration of the N-type dopant.

a1

9. (currently amended) The charge pump circuit of claim ~~8~~ 2 further comprising:

~~a fourteenth transistor coupled to the thirteenth transistor;~~

~~a fourteenth capacitor coupled to the fourteenth transistor;~~

~~a fifteenth transistor coupled to the fourteenth transistor; and~~

~~an fifteenth capacitor coupled to the fifteenth transistor, wherein the fourteenth and fifteenth transistors each have a lower threshold voltages than the first transistor at a common source voltage~~

second capacitors, wherein a gate of each of the first and the second depletion transistors and the first native transistor is coupled to one of the second capacitors, a first subset of the second capacitors are coupled to receive a third clock signal, and a second subset of the second capacitors are coupled to receive a fourth clock signal.

Claim 10. (currently amended) The charge pump circuit of claim ~~3~~ ~~wherein the first and third capacitors are coupled to receive a first clock signal, and the second and fourth capacitors are coupled to receive a second clock signal~~ 1 further comprising:

a second native transistor coupled to a gate, a drain, and a source of the first native transistor; and

third native transistors, wherein a gate, the drain, and a source of each of the first depletion transistors are coupled to one of the third native transistors.

Claim 11 (canceled).

12. (currently amended) A method for receiving an input voltage and providing a boosted output voltage, the method comprising:

~~increasing a first voltage at a first capacitor;~~

~~coupling the first capacitor to a second capacitor through a first transistor;~~

~~increasing a second voltage at the second capacitor; and~~

~~coupling the second capacitor to a third capacitor through a second depletion transistor~~

boosting the input voltage by applying a first clock signal to a drain of a first native transistor; and

boosting a source voltage of the first native transistor by applying the first clock signal and a second clock signal to a drain and a source of each of a first set of depletion transistors that are coupled together in series to provide an output voltage,

the first set of depletion transistors each having a threshold voltage that is lower that a threshold voltage of the first native transistor at a common source voltage.

13. (currently amended) The method of claim 12 further comprising:

~~increasing a third voltage at the third capacitor;~~

~~coupling the third capacitor to a fourth capacitor through a third depletion transistor;~~

~~increasing a fourth voltage at the fourth capacitor; and~~

~~coupling the fourth capacitor to a fifth capacitor through a fourth deletion transistor~~

boosting the output voltage of the first native transistors by applying the first clock signal and the second clock signal to a drain and a source of each of a second set of depletion transistors that are coupled together in series and to the first depletion transistors,

the second set of depletion transistors each having a threshold voltage that is lower than the threshold voltage of each of the first set of depletion transistors at a common source voltage.

14. (currently amended) The method of claim 13 ~~further comprising:~~

~~increasing a fifth voltage at the fifth capacitor;~~

~~coupling the fifth capacitor to a sixth capacitor through a fifth depletion transistor;~~

~~increasing a sixth voltage at the sixth capacitor; and~~

~~coupling the sixth capacitor to a seventh capacitor through a sixth depletion transistor~~

wherein the gate of each of the first and the second sets of depletion transistors and the first native transistor is coupled to receive a third clock signal or a fourth clock signal.

15. (currently amended) The method of claim 14 ~~further comprising:~~

~~increasing a seventh voltage at the seventh capacitor;~~

~~coupling the seventh capacitor to a eighth capacitor through a seventh depletion transistor;~~

~~increasing an eighth voltage at the eighth capacitor; and~~

~~coupling the eighth capacitor to a ninth capacitor through a eighth depletion transistor~~

wherein the first set of depletion transistors includes at least four depletion transistors, and the second set of depletion transistors includes at least four depletion transistors.

16. (currently amended) The method of claim 15 ~~further comprising:~~

~~increasing a ninth voltage at the ninth capacitor;~~

~~coupling the ninth capacitor to a tenth capacitor through a ninth depletion transistor;~~

~~increasing a tenth voltage at the tenth capacitor; and~~

~~coupling the tenth capacitor to an eleventh capacitor through a tenth depletion transistor~~

wherein the first set of depletion transistors includes at least six depletion transistors, and the second set of depletion transistors includes at least six depletion transistors.

17. (currently amended) The method of claim 16 ~~further comprising:~~

~~increasing an eleventh voltage at the eleventh capacitor;~~

~~coupling the eleventh capacitor to a twelfth capacitor through an eleventh depletion transistor;~~

~~increasing a twelfth voltage at the twelfth capacitor; and~~

~~coupling the twelfth capacitor to a thirteenth capacitor through a twelfth depletion transistor~~

wherein the first set of depletion transistors includes at least seven depletion transistors, and the second sert of depletion transistors includes at least seven depletion transistors.

18. (currently amended) The method of claim 14 wherein ~~the first transistor has a greater threshold voltage than the second, third, fourth, fifth and sixth transistors at a common source voltage~~ each of the first set of depletion transistors has a negative threshold voltage implant region with a first concentration of dopant, and each of the second set of depletion transistors has a negative threshold implant region with a second concentration of dopant, the second concentration of dopant being greater than the first concentration of dopant.

Claim 19. (currently amended) The method of claim 13 ~~further comprising~~ wherein:

~~providing a first clock signal to the first and third capacitors; and~~

~~providing a second clock signal to the second and the fourth capacitors~~

a second native transistor is coupled to a gate, a drain, and source of the first native transistor; and

third native transistors that are each coupled to a gate, the drain, and the source of one of the first and the second sets of depletion transistors.

Claim 20 (canceled).

21. (currently amended) A charge pump circuit comprising:

~~a first stage comprising~~ a first ~~depletion~~ native ~~field-effect~~ transistor;

~~a second stage comprising a second~~ first depletion ~~field-effect transistor~~ transistors ~~the second stage being coupled to the first stage~~ each having a threshold voltage that is lower that a threshold voltage of the first native transistor at a common source voltage;

~~a first capacitor coupled to the first stage; and~~

~~a second capacitor coupled to the second stage~~

second depletion transistors each having a threshold voltage that is lower than the threshold voltage of each of the first depletion transistors at a common source voltage, wherein the first native transistor, the first depletion transistors, and the second depletion transistors are all coupled in series between an input and an output of the charge pump circuit;

first capacitors that are each coupled to a first clock signal and to the first and the second depletion transistors; and

second capacitors that are each coupled to a second clock signal and to the first and the second depletion transistors.

22. (currently amended) The charge pump circuit of claim 21 ~~further comprising:~~

~~a third stage comprising a third depletion field effect transistor, the third stage being coupled to the second stage;~~

~~a fourth stage comprising a fourth depletion field effect transistor, the fourth stage being coupled to the third stage;~~

~~a third capacitor coupled to the third stage; and~~

~~a fourth capacitor coupled to the fourth stage~~

wherein the first and second clock signals are HIGH concurrently for a fraction of a clock period.

Q1

23. (currently amended) The charge pump circuit of claim 22 further comprising:

~~a fifth stage comprising a fifth depletion field effect transistor, the fifth stage being coupled to the fourth stage;~~

~~a sixth stage comprising a sixth depletion field effect transistor, the sixth stage being coupled to the fourth stage;~~

~~a fifth capacitor coupled to the fifth stage; and~~

~~a sixth capacitor coupled to the sixth stage~~

third and fourth capacitors that are coupled to gates of alternating ones of the first and the second depletion transistors.

24. (currently amended) The charge pump circuit of claim 23 ~~further comprising:~~

~~a seventh stage comprising a seventh depletion field effect transistor, the seventh stage being coupled to the sixth stage;~~

~~an eighth stage comprising an eighth depletion field effect transistor, the eighth stage being coupled to the seventh stage;~~

~~a seventh capacitor coupled to the seventh stage; and~~

~~an eighth capacitor coupled to the eighth stage~~

wherein the third capacitors are coupled to receive a third clock signal, the fourth capacitors are coupled to receive a fourth clock signal, and the third and the fourth clock signals having non-overlapping HIGH pulses.

25. (currently amended) The charge pump circuit of claim ~~24~~ 21 ~~further comprising:~~

~~a ninth stage comprising a ninth field-effect transistor, the ninth stage being coupled to the eighth stage;~~

~~a tenth stage comprising a tenth depletion field-effect transistor, the tenth stage being coupled to the ninth stage;~~

~~an eleventh stage comprising an eleventh field-effect transistor, the eleventh stage being coupled to the tenth stage;~~

~~a ninth capacitor coupled to the ninth stage;~~

~~a tenth capacitor coupled to the tenth stage; and~~

~~an eleventh capacitor coupled to the eleventh stage~~

wherein the first depletion transistors include at least four depletion transistors, and the second depletion transistors include at least four depletion transistors.

26. (currently amended) The charge pump circuit of claim ~~22~~ 21 wherein ~~the first and third capacitors are coupled to receive a first clock signal, and the second and fourth capacitors are coupled to receive a second clock signal~~ the first depletion transistors include at least six depletion transistors, and the second depletion transistors include at least six depletion transistors.

27. (currently amended) The charge pump circuit of claim ~~26~~ 21 further comprising:

~~a fifth capacitor coupled to a gate of the first depletion transistor;~~

~~a sixth capacitor coupled to a gate of the second depletion transistor;~~

~~a seventh capacitor coupled to a gate of the third depletion transistor; and~~

~~an eighth capacitor coupled to a gate of the fourth depletion transistor, wherein the fifth and seventh capacitors are coupled to receive a third clock signal, and the sixth and eighth transistors are coupled to receive a fourth clock signal~~

a second native transistor that is coupled in series with the first native transistor.

28. (currently amended) The charge pump circuit of claim ~~27~~ 21 further comprising:

~~a fifth transistor coupled across two terminals of the first transistor and to the first capacitor;~~

~~a sixth transistor coupled across two terminals of the second transistor and to the second capacitor;~~

~~a seventh transistor coupled across two terminals of the third transistor and to the third capacitor; and~~

~~an eighth transistor coupled across two terminals of the fourth transistor and to the fourth capacitor~~

a second native transistor coupled to a gate, a drain, and source of the first native transistor; and

third native transistors that are each coupled to a gate, a drain, and a source of one of the first and the second depletion transistors.

29. (canceled).